

Post-Silicon And Runtime Verification For Modern Processors By Ilya Wagner;Valeria Bertacco

By Ilya Wagner;Valeria Bertacco

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International Conference on Runtime Verification (RV), 2011 Post-Silicon Fault Localisation Using Maximum Runtime Validation of Transactional

<http://www.ee.princeton.edu/people/faculty/sharad-malik>

1 Post-Silicon Verification under Limited Observability Ganesh 10 Potential Carry-over of Techniques Runtime verification of distributed embedded systems

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Technical Programme Committee; DATE post-silicon verification; online checkers and runtime verification targeting new and traditional architectures and

<http://www.date-conference.com/group/tpc/members/2016/D3>

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http://www.eecs.umich.edu/courses/eecs578/eecs578.w14_old/projects/team3_report.pdf

where different pre- and post-silicon techniques Ilya Wagner and Valeria Bertacco design verification, where different pre- and post-silicon

<http://citeseerx.ist.psu.edu/viewdoc/summary?doi=10.1.1.217.1632>

Adaptive RF Front-Ends for Hand-held Applications. Post-Silicon and Runtime Verification for Modern Processors, von: Ilya Wagner, Valeria Bertacco,

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Researching post-silicon and runtime verification - Researched pre- and post-silicon verification techniques for modern Ilya Wagner and Valeria Bertacco.

<https://www.linkedin.com/pub/dir/ilya/wagner>

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